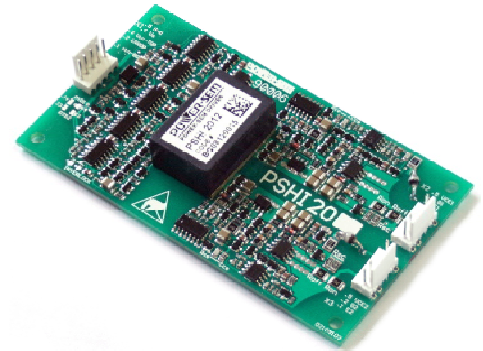


1. Absolute Maximum Ratings(Ta=25°C)

Symbol	Terms	Values	Units
V _S	Supply voltage primary	18	V
V _{iH}	Input signal voltage(HIGH)	V _S +0.3	V
I _{outPEAK}	Output peak current	±8	A
I _{outAV}	Output average current	±36	mA
V _{CE}	Collector-emitter voltage sense	1200 / 1700	V
dv/dt	Rate of rise and fall of voltage	75	kV/μs
V _{isol IO}	Isolation test volt.IN-OUT(1min.AC)	4000	V
R _{Gon min}	Minimal R _{Gon}	2.7	Ω
R _{Goff min}	Minimal R _{Goff}	2.7	Ω
Q _{out/pulse}	Charge per pulse	6.3	μC
T _{op}	Operating temperature	-25~85	°C
T _{stg}	Storage temperature	-25~85	°C



POWER-SEM PCB IGBT Driver PSHI 2012 PSHI 2017

High Power Double IGBT Driver

2. Electrical Characteristics

Symbol	Terms	Values			Unit
		min	typ	max	
V _S	Supply voltage primary	14.4	15	15.6	V
I _S	Supply current(max.)		0.3 ¹⁾		A
I _{SO} ²⁾	Supply current primary side(standby)		0.09		A
V _{IT+}	Input threshold voltage(HIGH)min For 15V input level	12.5			V
V _{IT-}	Input threshold voltage(LOW)max For 15V input level			3.6	V
R _{in}	Input resistance		10		kΩ
V _{G(on)}	Turn-on output gate voltage		15		V
V _{G(off)}	Turn-off output gate voltage		-8		V
f	Maximum operating frequency		see Fig.1		
t _{d(on)IO}	Input-output turn-on propagation time		1.4		μs
t _{d(off)IO}	Input-output turn-off propagation time		1.4		μs
t _{d(err)}	Error input-output propagation time		1 ³⁾		μs
V _{CEstat}	Reference voltage for V _{CE} monitoring		5.2 ⁴⁾ /6.3 ⁵⁾		V
C _{PS}	Primary to secondary capacitance		12		Pf

- 1) This current value is a function of the output load condition
- 2) Operating fsw=0Hz
- 3) This value is not considered by t_{on} and t_{dead} of IGBT, but adjusted by R_{CE} and C_{CE}
- 4) With R_{CE}=18k Ω, C_{CE}=330pF(PSHI2012 used for 1200V IGBT)
- 5) With R_{CE}=36k Ω, C_{CE}=470pF(PSHI2017 used for 1700V IGBT)

Features

- PSHI 20/12 drives all series IGBTs with V_{CES} up to 1200V(V_{CE}-monitoring adjusted from factory for 1200V IGBT)
- PSHI 20/17 drives all series IGBTs with V_{CES} up to 1700V(V_{CE}-monitoring adjusted from factory for 1700V IGBT)
- Double driver circuit for medium power IGBTs, also as two independent single drives
- CMOS level (15V) compatible input buffers
- Short circuit protection by V_{CE} monitoring
- Soft short circuit turn-off
- Isolation due to transformers(no opto couplers)
- Supply undervoltage protection(<13V)
- Error memory/output low level active
- Driver interlock top/bottom in half-bridge mode
- Internal isolated power supply
- Short-pulse control function

Typical Applications

- Single and bridge circuit
- Inverter
- Welding machine
- High power UPS
- High frequency SMPS

3. Product Overview

The new intelligent economically double IGBT driver, PSHI2012 respectively PSHI2017 is a standard driver for all power IGBTs in the market, they drive all IGBTs with V_{CE} up to 1200V and 1700V. (see Fig.1)

To protect the driver against moisture, dust and salt fog, it is coated with three-proof protective agents. It can drive dual IGBTs under half-bridge mode or independent mode. The high drive capability was designed to make it possible to switch up to 100A IGBT modules at frequencies up to 20kHz.

A new function has been added to the short circuit protection circuit (Soft Turn Off), this automatically increases the IGBT turn off time and hence reduces the DC voltage overshoot enabling the use of higher DC-bus voltages.

Integrated DC/DC converters with high galvanic isolation (4 kV/1 minute) ensures that the user is protected from the high voltage (secondary side). The power supply for the driver may be the same as used in the control board (0/+15V) without the requirement of isolation. All information that is transmitted between input and output uses ferrite transformers, resulting in high dv/dt immunity (75 kV/ μ s).

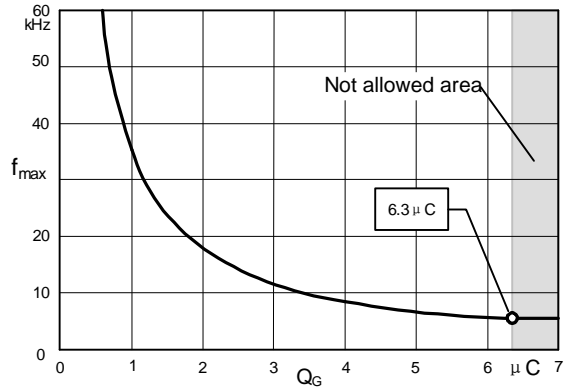


Fig.1 Relationship between maximum operating frequency and charge per pulse

4. Block diagram PSHI 20

Brief introduction to system structure and performance feature.

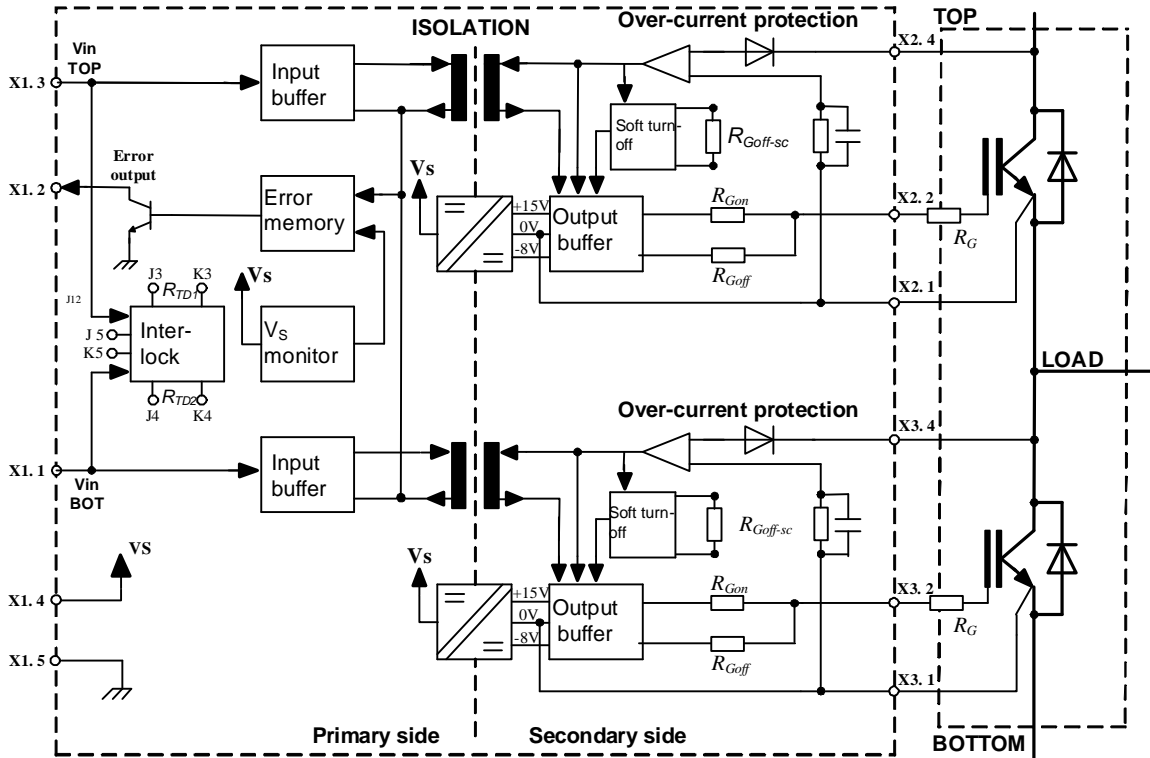


Fig.2 System structure of PSHI 20

- An “INTERLOCK” circuit prevents the two IGBTs of the half bridge to switch-on at the same time, and a “dead time”(default:10us) can be adjusted by adjusting resistor value of pins J3 & J3(R_{TD1}),and J4 & J4(R_{TD2}).Tab 1 shows the corresponding relationship between R_{TD} and dead time. The interlocking may also be inhibit by solder bridging between pins J5 and K5 to obtain two independent drivers.As pins J5 and K5 not bridged from factory, under half bridge mode, inter-lock function active.
- “INPUT BUFFER” circuit converts input signals in order to make them meet the needs of ferrite transformers and avoid other false signals being transmitted to output side.
- The “ERROR MEMORY” blocks the transmission of all turn-on signals to the IGBT and output error signal if either over-current or under-voltage is detected. Default error signal output is low level active.
- The “ V_s MONITOR” ensures that V_s actual is not below 13V.Once V_s below 13V, system will blocks the transmission of all input signals to the IGBT.
- With a “FERRITE TRANSFORMER” the information between primary and secondary may flow in both directions and high levels of dv/dt and high isolation voltage.At the same time, it can also restrain the short-pulse signals below 500ns.
- A high frequency “DC/DC power supply” used in “power output circuit” to supply isolation power supply with output voltage:+15V/-8V. Power supply use half-bridge circuit.The drivers and controlled system can use same power supply, even if we are using more than one PSHI20.
- In case of short-circuit, a further circuit (SOFT TURN-OFF) increases the resistance in series with R_{Goff} and turns-off the IGBT at a lower speed.This produces a smaller voltage spike above the DC link by reducing the di/dt value.Because in short-circuit conditions the Homogeneous IGBT's peak current increases up to 6-8 times the nominal current, and some stray inductance is always present in power circuits, it must fall to zero in a longer time than at normal operation to avoid damage IGBT by high voltage spike.The default resistor used for soft turn-off is 11Ω ,this “soft turn-off time” can be reduced by connecting a parallel resistor $R_{Goff-SC}$ with those already on the printed circuit board.
- “ V_{CE} monitoring circuit” is responsible for short-circuit sensing. Due to the direct measurement of V_{CEstat} on the IGBT's collector, it blocks the output buffer (through the soft turn-off circuit) in case of short-circuit and sends a signal to the ERROR memory on the primary side.

R_{TD} resistance value	Dead time
10 k Ω	0.9 μ s
22 k Ω	1.8 μ s
33 k Ω	2.5 μ s
47 k Ω	3.2 μ s
68 k Ω	4 μ s
100 k Ω	5 μ s
330 k Ω	7.7 μ s
not bridged	10 μ s

Tab 1.Corresponding relationship between R_{TD} and dead time

Attention:If this function is not used, for example during the experimental phase(not connect to IGBT), the V_{CE} MONITORING(X2.4;X3.4) must be connected with the EMITTER output(X2.1;X3.1) to avoid possible fault indication and consequent gate signal blocking.

- “The OUTPUT BUFFER” is responsible for providing +15V/-8V level from the DC/DC inverter, and enhance the control signal from the pulse transformer. The output stage has a MOSFET pair which is able to source/sink up to 8A peak current to/from the gate improving the turn-on/off capability.If these signals do not have sufficient power, the IGBT will not switch properly, and additional losses or even the destruction of the IGBT may occur. According to the application (switching frequency and gate charge of the IGBT),different R_G must be selected. $R_{Gon}=R_{Goff}=1.2 \Omega$. There is no installed R_G , user can get need R_G by series relevant resistor on outer board.

Please make sure that the total value of R_G not below 2.7 Ω in order to avoid damaging driver.

5. Input Interface Criterion

1).Input Signal Level

Input PWM signals can be CMOS level,active-logic control(high level IGBT switch on).The following overview is showing the input threshold voltages:

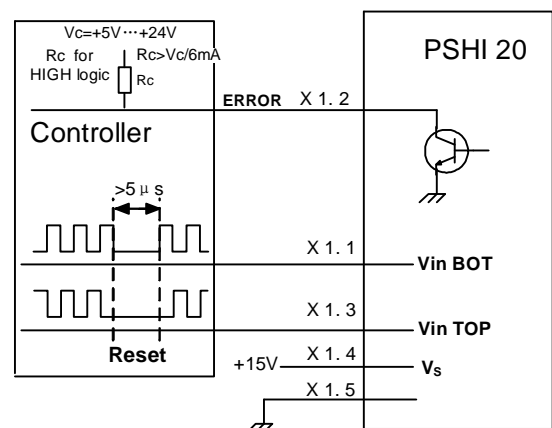


Fig.3 Connecting for input interface

15 V	min	typ	max
V_{IT+} (High)	9.5 V	11.0 V	12.5 V
V_{IT-} (Low)	0.50 V	0.65 V	0.80 V

X1.3 is up IGBT controlled signal, while X1.1 is bottom IGBT signal.

The installed pull-up resistor in drivés signal input stage, make sure the IGBT turn-off when inputs un-connected or un-bridged.

2).Error Output

When over-current occurs, driver can cut off IGBT automatically. Fault signals output (X1.2) is low level active.The outer board is not required to be connected through a pull-up resistor.

3).Error Reset

Install both X1.3 and X1.1 LOW at the same time for more than 5us, error reset automatically.

4).Connecting leads between Driver and Control Board

The length between driver and control board should be kept short.

6. Dimensions and connections of The PSHI 20

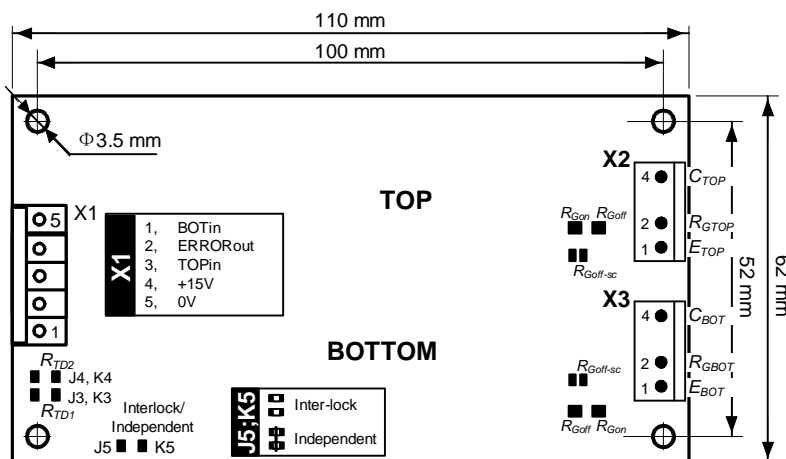


Fig.4 Installation dimensions and pins place instruction

Tab.2 Pins place instruction from J3,K3 to J18,K18

Function	Pin description	Adjustment by factory	Possibilities of functions
Dead time	J3,K3: TOP(R_{TD1}) J4,K4: BOT(R_{TD2})	not equipped; 10μs	adjustment according Tab.1
Inter-lock	J5,K5	not bridged; interlock	soldering bridged:Independent
$R_{Goff-SC}$ TOP		11Ω	adjustment automatically
$R_{Goff-SC}$ BOT		11Ω	adjustment automatically

7. Application/Handling

1).The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than ($V_{+0.3V}$) or under -0.3V may destroy drivers. Therefore, the signal of control board must be observed for above mentioned demand,and not-used pins should be soldering bridged with GND in order to avoid un-equipped pins. Pay more attention to electrostatic breakdown.

2).The connecting leads between the driver and the IGBT module must be as short as possible, and should be twisted.

3).Any parasitic inductance should be minimized, turn-off over-voltage can be decreased by differenet snubber circuit.

4).It is important to feed any ERROR back to the control circuit to switch the equipment off immediately in such events.

Repeated turn-on of the IGBT into a short circuit, with a frequency of several kHz, may destroy the device.